CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor device comprising a MOS transistor with a gate electrode,

wherein a dummy pattern is spaced away from both sides of the gate electrode,

a first silicide layer is formed in the upper portion of the gate electrode,

a second silicide layer is formed in a region between the gate electrode and the dummy pattern, and

the first silicide layer has a greater thickness than the second silicide layer.

2. A semiconductor device comprising a MOS transistor with a plurality of gate electrodes,

wherein each of the gate electrodes is arranged between the other gate electrodes or between one of the gate electrodes and a dummy pattern with a space left at each side thereof,

a first silicide layer is formed in the upper portion of the gate electrode,

a second silicide layer is formed in a region between the gate electrode and at least one of another gate electrode and the dummy pattern, and

the first silicide layer has a greater thickness than the second silicide layer.

3. The device of claim 1 or 2, wherein the dummy pattern is a dummy gate electrode which is an electrode pattern having the shape of a gate electrode, and the dummy pattern is an electrode which is not electrically connected to a semiconductor integrated circuit of the semiconductor device.

4. The device of claim 1 or 2, wherein the dummy pattern is made of insulating material.

5. The device of claim 1 or 2, wherein the dummy pattern is either a pattern made of insulating material or a dummy gate electrode which is an electrode pattern having the shape of a gate electrode and is not electrically connected to a semiconductor integrated

circuit of the semiconductor device.

6. The device of claim 4, wherein the MOS transistor is formed in an element region surround with an isolation insulating film, and

the pattern made of insulating material is formed on the isolation insulating film.

7. The device of claim 5, wherein the MOS transistor is formed in an element region surround with an isolation insulating film, and

the pattern made of insulating material is formed on the isolation insulating film.

8. The device of claim 1 or 2, wherein the thickness of the second silicide layer is 80% or less of the thickness of the first silicide layer.

9. The device of claim 1 or 2, wherein the MOS transistor is formed in an element region surrounded with an isolation insulating film, and

the thickness of the second silicide layer or layers satisfies $2(TM - Tm) / (TM + Tm) < 0.3$, where TM and Tm are the maximum and minimum thicknesses of the second silicide layer or layers in the element region, respectively.

10. The device of claim 1 or 2, wherein the distance **A** from a side wall of the gate electrode to a side wall of another said gate electrode or a side wall of the dummy pattern adjacent to the gate electrode holds the relation: $A \leq 2B$ relative to the height **B** of the gate electrode.

11. The device of claim 10, wherein the MOS transistor is formed in an element region surrounded with an isolation insulating film,

the gate electrode comprises two portions extending substantially parallel to each other and a connecting portion connecting respective ends of the two portions to each other,

the connecting portion is located on the isolation insulating film, and

the distance **C** from the boundary between the isolation insulating film and the element region to the connecting portion holds the relation: $C \geq 2B$ relative to the gate electrode height **B**.

12. The device of claim 1 or 2, wherein the MOS transistor has a gate length of 0.15 μm or smaller.

13. The device of claim 1 or 2, wherein the first and second silicide layers contain one selected from the group consisting of $CoSi_x$, $TiSi_x$, $NiSi_x$, and $PtSi_x$, and x satisfies $0 < x \leq 2$.

14. A semiconductor device comprising a MOS transistor with a plurality of gate electrodes,

wherein the gate electrodes are formed on a semiconductor substrate having a silicon layer at least in the surface thereof,

the MOS transistor has a gate length of 0.15 μm or smaller and is formed in an element region surrounded with an isolation insulating film,

each of the gate electrodes is arranged between the other gate electrodes or between one of the other electrodes and a dummy pattern with a space left from each side thereof,

sidewalls are provided on side walls of each of the gate electrodes and on side walls of another said gate electrode,

a first silicide layer is formed in the upper portion of the gate electrode,

a second silicide layer is formed in a portion of the semiconductor substrate surface which is located in part of the element region between the gate electrode and at least one of another gate electrode and the dummy pattern, and

the first silicide layer has a greater thickness than the second silicide layer.

15. The device of claim 14, wherein the dummy pattern is a dummy gate electrode which is an electrode pattern having the shape of a gate electrode, side walls of the dummy pattern are provided with sidewalls, and the dummy pattern is an electrode which is not electrically connected to a semiconductor integrated circuit of the semiconductor device.

16. The device of claim 14, wherein the dummy pattern is made of insulating material.

17. The device of claim 14, wherein the dummy pattern is either a pattern made of

insulating material or a dummy gate electrode which is an electrode pattern having the shape of a gate electrode with side walls of the dummy pattern provided with sidewalls and is not electrically connected to a semiconductor integrated circuit of the semiconductor device.

18. The device of claim 16 or 17, wherein the pattern made of insulating material is formed on the isolation insulating film.

19. A method for fabricating a semiconductor device, comprising the steps of:

forming a gate insulating film on a semiconductor substrate having a silicon layer at least in the surface thereof, and depositing an amorphous silicon film or a polysilicon film on the gate insulating film;

patterning the amorphous silicon film or the polysilicon film to form a gate electrode and at least one of another gate electrode and a dummy gate electrode, at least one said electrode being spaced away from both sides of the gate electrode;

doping impurities into the semiconductor substrate to form doped layers serving as a source and a drain; and

depositing a metal film on the semiconductor substrate, the gate electrode, and another said gate electrode or the dummy gate electrode, and performing heat treatment on the metal film, thereby forming silicide on the semiconductor substrate, the gate electrode, and at least one electrode of another said gate electrode and the dummy gate electrode.

20. The method of claim 19, further comprising the step of forming sidewalls on side walls of the gate electrode and on side walls of at least one electrode of another said gate electrode and the dummy gate electrode.

21. A method for fabricating a semiconductor device, comprising the steps of:

forming a gate insulating film on a semiconductor substrate having a silicon layer at least in the surface thereof, and depositing an amorphous silicon film or a polysilicon film on the gate insulating film;

patterning the amorphous silicon film or the polysilicon film to form a plurality of

aligned gate electrodes in array form;

doping impurities into the semiconductor substrate to form doped layers serving as a source and a drain;

depositing an insulating layer on the semiconductor substrate;

patterning the insulating layer to form dummy patterns disposed away from both sides of the electrode array in the alignment direction thereof, respectively; and

depositing a metal film on the semiconductor substrate, the gate electrode, and the dummy patterns, and performing heat treatment on the metal film, thereby forming silicide on the semiconductor substrate and the gate electrode.

22. A method for fabricating a semiconductor device, comprising the steps of:

forming an isolation insulating film on a semiconductor substrate having a silicon layer at least in the surface thereof, to form an element region surrounded with the isolation insulating film;

forming a gate insulating film on the semiconductor substrate, and depositing an amorphous silicon film or a polysilicon film on the gate insulating film;

patterning the amorphous silicon film or the polysilicon film to form a gate electrode on the element region and form a dummy gate electrode disposed on the isolation insulating film and adjacent to the gate electrode;

doping impurities into the semiconductor substrate to form doped layers serving as a source and a drain;

depositing an insulating layer on the semiconductor substrate;

patterning the insulating layer to form a dummy pattern disposed on the isolation insulating film and adjacent to the gate electrode; and

depositing a metal film on the semiconductor substrate, the gate electrode, the dummy gate electrode, and the dummy pattern, and performing heat treatment on the metal film, thereby forming silicide on the semiconductor substrate, the gate electrode, and the dummy gate electrode.

23. The method of claim 22, further comprising the step of forming sidewalls on side walls of the gate electrode and on side walls of the dummy gate electrode.

24. The method of claim 19 through 23, wherein the metal film contains one selected from the group consisting of Co, Ti, Ni, and Pt.

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